

## CLAIMS

What is claimed is:

- 1        1.        A method comprising:  
2                applying a first predetermined signal to a first wire;  
3                applying a second predetermined signal to a second wire, wherein the second wire  
4                is parallel to the first wire; and  
5                determining, based at least in part on a current signal, a cross coupling capacitance  
6                between the first wire and the second wire.
- 1        2.        The method of claim 1 wherein the second predetermined signal comprises  
2                a constant voltage for a first period of time and a periodic signal for a second period of  
3                time.
- 1        3.        The method of claim 1 wherein applying a first predetermined signal to the  
2                first wire further comprises:  
3                applying a first periodic voltage to a first transistor; and  
4                applying a second periodic voltage to the first wire via an inverter.
- 1        4.        The method of claim 3 wherein the current signal corresponds to current  
2                flowing through the first transistor.

1 5. A machine readable storage medium having stored therein a plurality of  
2 machine executable instructions that implement a parasitic extraction tool that operates to  
3 generate electrical modeling data for an integrated circuit (IC) design, wherein the  
4 parasitic extraction tool includes a database of capacitance values, wherein the  
5 capacitance values are determined by:

6 evaluating a first predetermined signal on a first wire;  
7 evaluating a second predetermined signal on a second wire; and  
8 determining, based at least in part on a current signal, a cross coupling capacitance  
9 between the first wire and the second wire.

1 6. The machine readable medium of claim 5 wherein the second  
2 predetermined signal comprises a constant voltage for a first period of time and a periodic  
3 signal for a second period of time.

1 7. The machine readable medium of claim 5 further comprising determining,  
2 based at least in part on the current signal, a total capacitance of the first wire.

1 8. The machine readable medium of claim 5 wherein a first predetermined  
2 signal on the first wire comprises:

3 evaluating a first periodic current voltage to the first wire via a transistor; and  
4 evaluating a second periodic current voltage to the first wire via an inverter.

1 9. The machine readable medium of claim 8 wherein the current signal  
2 corresponds to current flowing through the transistor.

1 10. A machine readable storage medium having stored therein a plurality of  
2 machine executable instructions that implement an integrated circuit (IC) design  
3 simulation tool, wherein the IC design tool simulates an IC design based on capacitance  
4 values determined by:  
5 evaluating a first predetermined signal on a first wire;  
6 evaluating a second predetermined signal on a second wire; and  
7 determining, based at least in part on a current signal, a cross coupling capacitance  
8 between the first wire and the second wire.

1 11. The machine readable medium of claim 10 wherein the second  
2 predetermined signal comprises a constant voltage for a first period of time and a periodic  
3 signal for a second period of time.

1 12. The machine readable medium of claim 10 further comprising  
2 determining, based at least in part on the current signal, a total capacitance of the first  
3 wire.

1 13. The machine readable medium of claim 10 wherein a first predetermined  
2 signal on the first wire comprises:  
3 evaluating a first periodic current voltage to the first wire via a transistor; and

4 evaluating a second periodic current voltage to the first wire via an inverter.

1 14. The machine readable medium of claim 13 wherein the current signal  
2 corresponds to current flowing through the transistor.

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